IN THE CLAIMS

1. (Previously Presented) A method for providing a response to a cache access request, the method comprising:

receiving a cache access request associated with a memory line at a cache coherence controller from a processor in a cluster of processors, the cluster of processors interconnected in a point-to-point architecture;

obtaining response information for the cache access request from a remote data cache associated with the cache coherence controller;

determining that the cache access request can be handled locally by using the remote data cache without having to probe remote nodes; and

providing response information with a completion indicator to the processor when it is determined that the cache access request can be handled locally.

2. (Previously Presented) The method of claim 1, wherein the cache access request can be handled locally if a valid copy of the memory line is in the remote data cache.

3. (Original) The method of claim 1, wherein response information includes state information.

4. (Previously Presented) The method of claim 2, wherein the completion indicator is a completion bit.

5. (Original) The method of claim 1, wherein the completion indicator notifies the processor that the response from the cache coherence controller will be the only response.

6. (Original) The method of claim 1, wherein the processor is a request processor in a request cluster.

7. (Original) The method of claim 1, wherein the completion indicator allows the cache coherence controller to avoid probing local or remote nodes.

8. (Original) The method of claim 1, wherein the processor sends a source done upon identifying the completion indicator in the response.

9. (Original) The method of claim 8, wherein the processor sends the source done to the cache coherence controller.

10. (Original) The method of claim 9, wherein the processor sends the source done to the cache coherence controller acting as a memory controller.

11. (Previously Presented) A processing cluster, comprising:

a plurality of processors interconnected in a point-to-point architecture;

a cache coherence controller configured to receive a cache access request associated with a memory line from a first processor amongst the plurality of processors, obtain response information for the cache access request from a remote data cache associated with the cache coherence controller and provide response information with a completion indicator to the processor if it is determined that a valid copy of the memory line is in the remote data cache.

12. (Original) The processing cluster of claim 11, wherein response information is provided in a response packet.

13. (Original) The processing cluster of claim 11, wherein response information includes state information.

14. (Original) The processing cluster of claim 12, wherein response information includes data.

15. (Original) The processing cluster of claim 11, wherein the completion indicator notifies the first processor that the response from the cache coherence controller will be the only response.

16. (Original) The processing cluster of claim 11, wherein the first processor is a request processor in a request cluster.

17. (Original) The processing cluster of claim 11, wherein the completion indicator allows the cache coherence controller to avoid probing local or remote nodes.

18. (Original) The processing cluster of claim 11, wherein the first processor sends a source done upon identifying the completion indicator in the response.

19. (Original) The processing cluster of claim 18, wherein the first processor sends the source done to the cache coherence controller.

20. (Previously Presented) A cache coherence controller, comprising:

means for receiving a cache access request associated with a memory line at a cache coherence controller from a processor in a cluster of processors, the cluster of processors interconnected in a point-to-point architecture;

means for obtaining response information for the cache access request from a remote data cache associated with the cache coherence controller; and

means for providing response information with a completion indicator to the processor after determining that the cache access request can be completed locally.